E-QSFP28-IR4

100GBASE-CWDM4 QSFP28 1310nm 2km DDM SMF Transceiver

Features

- Supports103.1Gb/s, each lane bit rate 25.78 Gb/s
- Up to 2km transmission on single mode fiber (SMF) with FEC
- LAN WDM DFB laser and PIN receiver
- I2C interface with integrated Digital Diagnostic monitoring
- QSFP28 MSA package with duplex LC connector
- Single +3.3V power supply
- 4 CWDM lanes MUX/DEMUX design
- 100G CWDM4 MSA Technical Spec Rev1.1
- Maximum power consumption 3.5W
- Operating case temperature: 0 to +70°C
- Complies with EU Directive 2011/65/EU (RoHS 6/6)

Application

- Data Center Interconnect
- 100G Ethernet
- Infiniband QDR and DDR interconnects
- Enterprise networking

1. Absolute Maximum Ratings

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Storage Temperature	TS	-40	-	+85	°C	
Supply Voltage	VCC	-0.5	-	+4.0	V	
Operating Relative Humidity	RH	-	-	+85	%	

2. Recommended Operating Conditions

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Operating Case Temperature	TC	0	-	+70	°C	
Power Supply Voltage	VCC	3.13	3.3	3.47	V	
Power Supply Current	ICC	-	-	1.06	A	
Maximum Power Dissipation	PD	-	-	3.5	W	
Aggregate Bit Rate	BRAVE	-	103.125	-	Gb/s	

Lane Bit Rate	BRLANE	-	25.78	-	Gb/s	
Transmission Distance	TD		-	2	km	Over SMF

3. Digital Diagnostics

Parameter	Range	Accuracy	Unit	Calibration
Temperature	0 to 70	±3	ºC	Internal
Voltage	0 to VCC	0.1	V	Internal
TxBias CurrentPer Lane	0 to 100	10%	mA	Internal
Tx Output Power Per Lane	to 2.9	±3	dBm	Internal
Rx Power (Each Lane)	-21 to 5	±3	dBm	Internal

4. Optical Characteristics

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Transmitter						
Center Wavelength Lane 0	λ0	1264.5	1271	1277.5	nm	
Center Wavelength Lane 1	λ1	1284.5	1291	1297.5	nm	
Center Wavelength Lane 2	λ2	1304.5	1311	1317.5	nm	
Center Wavelength Lane 3	λ3	1324.5	1331	1337.5	nm	
Total Launch Power	PALL	-	-	8.5	dBm	1
Average Launch Power per Lane	PTX_LANE	-6.5	-	2.5	dBm	1
Optical Modulation Amplitude (OMA), each Lane	POMA	-4		2.5	dBm	1
Launch Power in OMA minus Transmitter and Dispersion Penalty (TDP), each Lane		-5			dBm	
TDP, each Lane	TDP		-	3	dBm	
Extinction Ratio	ER	3.5	-	-	dB	
Relative Intensity Noise	RIN		-	-130	dB/Hz	12dB reflection
Optical Return Loss Tolerance	TOL		-	20	dB	2
Transmitter Reflectance	RT		-	12	dB	
Average Launch Power OFF Transmitter, each Lane	Poff		-	-30	dBm	2
Transmitter Eye Mask Definition {X1, X2, X3, Y1, Y2, Y3}		{0.31, 0.4, 0.45, 0.34, 0.38, 0.4}				2
Receiver						
Damage Threshold, each Lane	THd	3.5			dBm	3
Total Average Receive				8.5	dBm	

Power						
Average Receive Power, each Lane		-11.5		2.5	dBm	
Receive Power (OMA), each Lane				2.5	dBm	
Receiver Sensitivity (OMA), each Lane	SEN			-11.5	dBm	for BER = 5x10-5
Stressed Receiver Sensitivity (OMA), each Lane				-7.3	dBm	4
Receiver Reflectance	RR			-26	dB	
LOS Assert	LOSA	-30			dBm	
LOS Deassert	LOSD			-12	dBm	
LOS Hysteresis	LOSH	0.5			dB	
Receiver Electrical 3 dB upper Cutoff Frequency, each Lane				31	GHz	
Conditions of Stress Receiver Sensitivity Test (Note 5)						
Vertical Eye Closure Penalty, each Lane			1.9		dB	
Stressed Eye J2 Jitter, each Lane			0.33		UI	
Stressed Eye J4 Jitter, each Lane			0.48		UI	
SRS eye mask definition { X1, X2, X3, Y1, Y2, Y3}		{0.39, 0.5, 0.5, 0.39, 0.39, 0.4}				

Notes:

1. Even if the TDP < 1.0 dB, the OMA min must exceed the minimum value specified here.

2. Hit ratio 5x10-5.

3. The receiver shall be able to tolerate, without damage, continuous exposure to a modulated optical input signal having this power level on one lane. The receiver does not have to operate correctly at this input power.

4. Measured with conformance test signal for BER = 5x10-5.

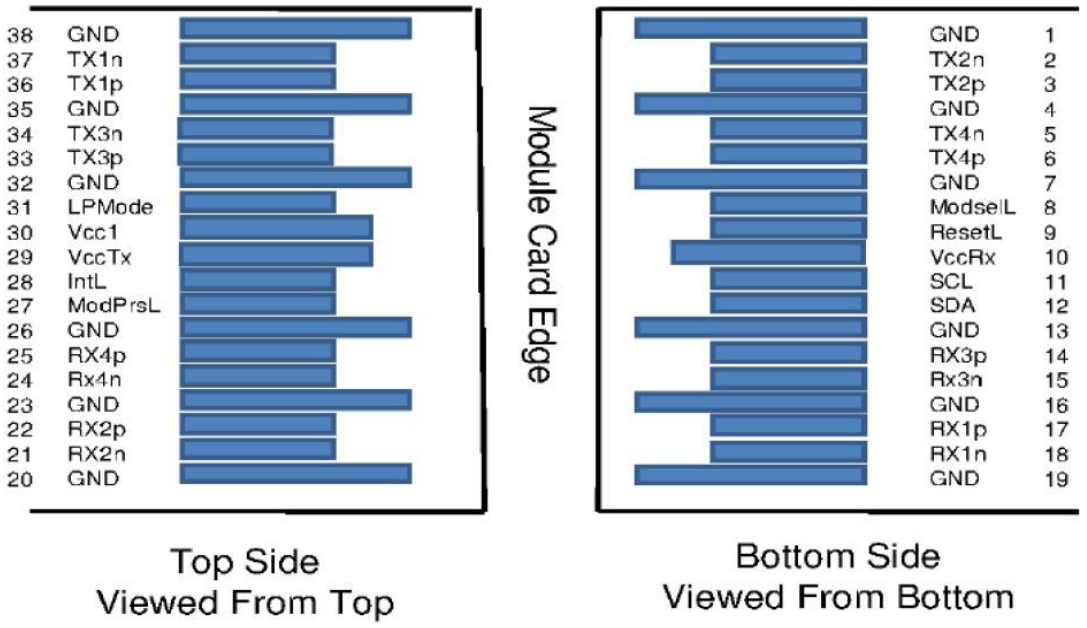
5. Vertical eye closure penalty, stressed eye J2 jitter, stressed eye J4 jitter, and SRS eye mask definition are test conditions for measuring stressed receiver sensitivity. They are not characteristics of the receiver

5. Electrical Characteristics

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Transmitter (Module Input)						
Differential Data Input Amplitude	VIN,P-P	100	-	1100	mVpp	
Input Impedance (Differential)	ZIN	85	100	115	Ohms	
Differential Termination Mismatch		-	-	10	%	
Receiver (Module Output)						
Differential Data Output Amplitude	VOUT,P-P	200	-	900	mVpp	
Output Impedance (Differential)	ZOUT	85	100	115	Ohms	
Differential Termination Mismatch		-	-	10	%	

Output Rise/Fall Time, 20%~80%	TR/TF	12	-	-	ps	

6. Pin Description



7. Pin Definition

Pin	Name	Logic	Function	Plug Seq.	Notes
1	GND		Ground	1	1
2	Tx2n	CML-I	Transmitter Inverted Data Input	3	
3	Tx2p	CML-I	Transmitter Non-Inverted Data Input	3	
4	GND		Ground	1	1
5	Tx4n	CML-I	Transmitter Inverted Data Input	3	
6	Tx4p	CML-I	Transmitter Non-Inverted Data Input	3	
7	GND		Ground	1	1
8	ModSelL	LVTTL-I	Module Select	3	
9	ResetL	LVTTL-I	Module Reset	3	
10	VccRx		+3.3V Power Supply Receiver	2	2
11	SCL	LVCMOS-I/O	2-wire serial interface clock	3	
12	SDA	LVCMOS-I/O	2-wire serial interface data	3	
13	GND		Ground	1	
14	Rx3p	CML-O	Receiver Non-Inverted Data Output	3	
15	Rx3n	CML-O	Receiver Inverted Data Output	3	
16	GND		Ground	1	1
17	Rx1p	CML-O	Receiver Non-Inverted Data Output	3	
18	Rx1n	CML-O	Receiver Inverted Data Output	3	
19	GND		Ground	1	1
20	GND		Ground	1	1

21	Rx2n	CML-O	Receiver Inverted Data Output	3	
22	Rx2p	CML-O	Receiver Non-Inverted Data Output	3	
23	GND		Ground	1	1
24	Rx4n	CML-O	Receiver Inverted Data Output	3	
25	Rx4p	CML-O	Receiver Non-Inverted Data Output	3	
26	GND		Ground	1	1
27	ModPrsL	LVTTL-O	Module Present	3	
28	IntL	LVTTL-O	Interrupt	3	
29	VccTx		+3.3V Power supply transmitter	2	2
30	Vcc1		+3.3V Power supply	2	2
31	LPMode	LVTTL-I	Low Power Mode	3	
32	GND		Ground	1	1
33	Tx3p	CML-I	Transmitter Non-Inverted Data Input	3	
34	Tx3n	CML-I	Transmitter Inverted Data Input	3	
35	GND		Ground	1	1
36	Tx1p	CML-I	Transmitter Non-Inverted Data Input	3	
37	Tx1n	CML-I	Transmitter Inverted Data Input	3	
38	GND		Ground	1	1

Notes:

1. GND is the symbol for signal and supply (power) common for QSFP28 modules. All are common within the QSFP28 module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal common ground plane.

2. VccRx, Vcc1 and VccTx are the receiving and transmission power suppliers and shall be applied concurrently.

3. Recommended host board power supply filtering is shown in Figure 3 below. Vcc Rx, Vcc1 and VccTx may be internally connected within the QSFP28 transceiver module in any combination. The connector pins are each rated for a maximum current of 1000mA.